Amendments to the Claims

Please replace all prior versions, and listings, of claims in the application with the following:

1. (Original) A temperature probe comprising:

a temperature sensor that provides a resistive output,

a logic circuit for determining a modified resistive output for the temperature sensor, and

a means for providing the modified resistive output.

2. (Original) The temperature probe of claim 1 wherein the logic circuit is programmed to execute a predictive or a correlative algorithm.

3. (Original) The temperature probe of claim 2 wherein the logic circuit is a microprocessor.

4. (Original) The temperature probe of claim 3 wherein the means for providing the modified resistive output is a potentiometer and the logic circuit sends a control signal to the potentiometer such that the potentiometer provides the modified resistive output.

5. (Original) The temperature probe of claim 3 wherein the means for providing the modified resistive output includes a FET.

6. (Original) The temperature probe of claim 3 wherein the means for providing the modified resistive output includes a photocell and a LED.

7. (Original) The temperature probe of claim 4 wherein the probe includes two potentiometers.

8. (Currently Amended) ~~A monitor~~ An interface for a monitor and a temperature probe including a temperature sensor comprising:

a logic circuit for determining a modified resistive output for the temperature sensor and

a means for providing the modified resistive output.

9. (Original) The interface of claim 8 wherein the logic circuit is programmed to execute a predictive or a correlative algorithm.

10. (Original) The interface of claim 9 wherein the logic circuit is a microprocessor.

11. (Original) The interface of claim 8 wherein the means for providing the modified resistive output is a potentiometer and the logic circuit sends a control signal to the potentiometer such that the potentiometer provides the modified resistive output.

12. (Original) The interface of claim 11 wherein the probe includes two potentiometers.

13. (Original) The interface of claim 8 wherein the means for providing the modified resistive output includes a FET.

14. (Original) The interface of claim 8 wherein the means for providing the modified resistive output includes a photocell and an LED.

15. (Currently Amended) The interface of claim 8 wherein the means for providing the modified resistive output ~~is a means for providing a modified resistive output~~ is compatible with the monitor such that the monitor can display a temperature that corresponds to the modified resistive output from the temperature probe.

16. (Previously Presented) A temperature probe comprising:

a temperature sensor having a resistive output,

a processor for determining a modified resistive output for the temperature sensor, the processor being programmed to execute a predictive or a correlative algorithm, and

a FET for providing the modified resistive output in response to a signal from the processor.

17. (Original) The temperature probe of claim 16 wherein the processor executes an algorithm to convert the resistive output of the temperature sensor to a modified resistive output that can be displayed by a monitor.

18. (Original) The temperature probe of claim 16 wherein the algorithm is a predictive algorithm that converts the resistive output of the temperature sensor during a thermally unstable condition to a modified resistive output representative of a predicted temperature during a condition of thermal stability.

19. (Previously Presented) The temperature probe of claim 16 wherein the probe includes two FETs.

20. (Original) An interface for converting the resistive output of a temperature sensor to a modified resistive output for display on a monitor comprising:

a logic circuit,

an input to the logic circuit from a temperature sensor,

an output from the logic circuit,

the logic circuit being programmed to execute a predictive or a correlative algorithm, and

a means for providing a resistance corresponding to the predicted or correlated output.

21. (Original) The interface of claim 20 wherein the resistive output from the temperature sensor is input to an analog to digital converter and the output from the analog to digital converter is fed to the logic circuit.

22. (Original) The interface of claim 20 wherein the logic circuit is a microprocessor.

23. (Original) The interface of claim 20 wherein the means for providing the resistance is a digital potentiometer and the microprocessor signals the potentiometer to assume a setting corresponding to the predicted output.

24. (Original) The interface of claim 23 wherein the interface includes two potentiometers.

25. (Previously Presented) A method for digitally modifying the resistive output of a temperature sensor which comprises inputting the resistive output from the temperature sensor to a logic circuit, implementing a predictive or a correlative algorithm using the logic circuit to determine a modified resistive output, controlling a gate of a FET to adopt a setting corresponding to the modified resistive output, and outputting a resistance corresponding to the modified resistive output.

26. (Previously Presented) The temperature probe of claim 5 wherein the probe includes two FETs.

27. (Previously Presented) The temperature probe of claim 5 wherein the microprocessor includes an output and the FET includes a gate, where the output of the microprocessor controls the gate of the FET such that the FET provides a FET resistance corresponding to the modified resistive output.

28. (Previously Presented) The temperature probe of claim 27 wherein the microprocessor further includes:

a first input from a first amplifier, where the first amplifier measures a FET voltage of the FET, and

a second input from a second amplifier, where the second amplifier measures a resistor voltage of a resistor having a first resistance,

where the microprocessor calculates a FET current using the first resistance and the resistor voltage from the second input, calculates a FET resistance using the FET voltage from the first input and the FET current, compares the FET resistance to the modified resistive output and applies a difference between the FET resistance and the modified resistive output as a negative feedback to the gate.

29. (Previously Presented) The interface of claim 13 wherein the interface includes two FETs.

30. (Previously Presented) The interface of claim 13 wherein the logic circuit includes an output and the FET includes a gate, where the output of the logic circuit controls the gate of the FET such that the FET provides a FET resistance corresponding to the modified resistive output.

31. (Previously Presented) The interface of claim 30 wherein the logic circuit further includes:

a first input from a first amplifier, where the first amplifier measures a FET voltage of the FET, and

a second input from a second amplifier, where the second amplifier measures a resistor voltage of a resistor having a first resistance,

where the logic circuit calculates a FET current using the first resistance and the resistor voltage from the second input, calculates a FET resistance using the FET voltage from the first input and the FET current, compares the FET resistance to the modified resistive output and applies a difference between the FET resistance and the modified resistive output as a negative feedback to the gate.

32. (Previously Presented) The temperature probe of claim 16 wherein the processor includes an output and the FET includes a gate, where the output of the processor controls the gate of the FET such that the FET provides a FET resistance corresponding to the modified resistive output.

33. (Previously Presented) The temperature probe of claim 32 wherein the processor further includes:

a first input from a first amplifier, where the first amplifier measures a FET voltage of the FET, and

a second input from a second amplifier, where the second amplifier measures a resistor voltage of a resistor having a first resistance,

where the processor calculates a FET current using the first resistance and the resistor voltage from the second input, calculates a FET resistance using the FET voltage from the first input and the FET current, compares the FET resistance to the modified resistive output and applies a difference between the FET resistance and the modified resistive output as a negative feedback to the gate.

34. (Previously Presented) The method of claim 25 further including measuring a FET voltage with a first amplifier, measuring a resistor voltage of a first resistor having a first resistance, calculating a FET current using the first resistance and the resistor voltage, calculating a FET resistance using the FET voltage and the FET current, comparing the FET resistance to the modified resistive output and applying a difference between the FET resistance and the modified resistive output as a negative feedback to the gate.